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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/895,306	AU ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *19 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-21* is/are allowed.

6)☒ Claim(s) *1 and 22-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 are pending.

Specification

2. The disclosure is objected to because of the following informalities: several minor typographic errors in specification.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature. **For example**, please change "read enables clock" on line 12 of page 5 to "read enable clock", and "embodiment fo the present invention" on line 22 of page 10 to "embodiment of the present information".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 29 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural

cooperative relationships are: the required input signals causing the means for generating a first latch and second latch outputs to generate said outputs in response.

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1 and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,994,920 to Narayana et al. (hereafter referred to as Narayana '920) in view of U.S. Patent 5,955,897 to Narayana et al. (hereafter referred to as Narayana '897).

8. As to claim 1, Narayana '920 discloses an apparatus receiving a first read clock (26), a first write clock (22), a first look-ahead signal (20), a second read clock (40), a second write clock (36), a second look-ahead signal (34) [col. 8, lines 20-30] to produce an output signal (HF) indicating if a FIFO is half-full or not half-full [col. 8, lines 32-33].

Narayana '920 also discloses a state machine (11) that is configured to receive a number of inputs including a look-ahead signal, a first and second read and write clock to produce an output signal indicating if a FIFO is half-full or not half-full [col. 6, lines 45-55]. Narayana '920 further discloses an apparatus that uses two state machines (12 &14), and a latch (16) to generate a FIFO half-full signal based on the input of a programmable look-ahead signal, and a first and second read and write clocks [col. 6, lines 58-67, and col. 7, lines 1-2].

Narayana '920 teaches all of the limitations, including a state machine that indicates when a FIFO is half-full and when said FIFO is not half-full, but does not teach that state machine indicates when a FIFO is almost full and when said FIFO is not almost full.

Narayana '897 teaches a state machine indicating a fullness of a FIFO similar to that of Narayana '920. In addition, Narayana '897 teaches that a state machine indicates when a FIFO is almost full and when said FIFO is not almost full [FIG. 3, and col. 3, lines 5-11]. Furthermore, Narayana '897 teaches that in addition to generating half-empty and half-full flags, it is well known in the art to generate programmable almost-full flags in a similar manner by adjusting an user programmable offset [col. 1, lines 15-24]. Thus, it would be obvious to one of ordinary skill in the art that the teachings of Narayana '920 could be modified from using half-full signals to use programmable almost-full signals, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the almost-full state machine as taught by Narayana '920. One of ordinary skill in the art would have been motivated to do so that the almost-fullness of the FIFO could be determined.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of using a state machine to determine a level within a FIFO. Moreover, the almost-full state machine means taught by Narayana '897 would improve the flexibility of Narayana '920 because it allowed for different levels within the FIFO to be determined in addition to the half-empty status, depending on the type of state machine used.

9. As to claim 22, Narayana '920 discloses a method for determining the emptiness of a memory buffer comprising: generating a half-full flag in response to a plurality of signals comprising a first and second read, write, and look-ahead signals [col. 8, lines 20-31]; generating a not half-full flag in response to same [col. 3, lines 4-6]; and presenting said signals to a state machine that generates an half-full flag [col. 8, lines 20-31]. Narayana '897 teaches that state machines indicating when a FIFO is almost full and when said FIFO is not almost full may likewise be used [col. 3, lines 5-11].

10. As to claim 23, Narayana '920 discloses that the generation of the fullness output flag is delayed by a time delay [col. 3, lines 51-54].

11. As to claim 24, Narayana '920 discloses that the generation of the not fullness output flag is delayed by a time delay [col. 3, lines 51-54]. Because Narayana '920 teaches that the not fullness output flag is generated at the same time as the fullness flag, a delay in the generation of the fullness flag also delays the not fullness flag.

12. As to claim 25 and 26, Narayana '920 discloses a programmable time delay in the generation of the fullness output flag and the not fullness output flag [col. 3, lines 51-54].

13. Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,994,920 to Narayana et al. (hereafter referred to as Narayana '920) in view of U.S. Patent

5,955,897 to Narayana et al. (hereafter referred to as Narayana '897), and in further view of U.S. Patent 5,231,314 to Andrews.

14. As to claims 27-28, Narayana '920 discloses that the delay block may be implemented either electronically or through discrete digital components without departing from the scope of the reference [col. 3, lines 54-58]. Thus Narayana '920 and Narayana '897 teach all of the limitations of the claim, but do not teach that the delay block may comprise a JTAG programmable delay block and other JTAG circuitry and instructions.

Andrews teaches that a JTAG programmable delay block may be used as a delay block in circuitry [col. 1, lines 41-53]. Thus, Andrews teaches a delay block similar to that of Narayana '920 and Narayana '897. Andrews further teaches that the delay block may be implemented as a JTAG programmable delay block, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the JTAG programmable delay block as taught by Andrews. One of ordinary skill in the art would have been motivated to do so to ensure reliable timing adjustment to compensate for clock skew [col. 1, lines 25-40].

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of implementing a timing delay block. Moreover, the JTAG programmable delay block means taught by Andrews would reduce the circuit complexity of Narayana '920 and Narayana '897 because it allowed for reliable timing without the need of separate set of test instrumentation [col. 1, lines 54-67].

Allowable Subject Matter

15. Claims 2-21 are allowed.

16. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record do not teach or suggest a synchronizer configured to generate a synchronized output signal in response to both a second set-output signal and a reset signal, within the construction of an apparatus, as claimed.

17. Claims 30-31 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

18. Applicant's arguments filed November 19, 2004 have been fully considered but they are not persuasive.

19. Applicant's arguments with respect to claims 1 and 22-31 have been considered but are moot in view of the new ground(s) of rejection.

20. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching,

suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

21. In the remarks, applicants argued in substance that the state machines taught by Narayana '920 and Narayana '897 are not similar. But Narayana '897 teaches that the state machine is similar to the state machine taught in co-pending U.S. Patent application 08/572,623, used to realize extremely short delays in generating half-full and half-empty flags [col. 1, lines 25-34]. Narayana '920 discloses that it is a continuation of U.S. Patent application 08/666,751, which is a continuation-in-part of U.S. Patent application 08/572,623 [col. 1, lines 4-7]. Thus there is some suggestion found in the references themselves to combine the teachings Narayana '920 and Narayana '897.

22. In the remarks, applicants argued in substance that Narayana '920 does not teach or suggest that the look-ahead signals are programmable and almost full signals. But Narayana '920 teaches that the signals 22 and 34 are look-ahead half-full signals [col. 2, lines 43-45 and col. 3, lines 14-24]. In addition, Narayana '897 teaches that in addition to generating half-empty and half-full flags, it is well known in the art to generate programmable almost-full flags in a similar manner by adjusting an user programmable offset [col. 1, lines 15-24]. Thus, it would be obvious to one of ordinary skill in the art that the teachings of Narayana '920 could be modified from using half-full signals to use programmable almost-full signals, substantially as claimed.

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

February 18, 2005
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